Parallelization of iterative solvers

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Convergence

Fixed grid 300×300, strong scalability

p increases

$\Downarrow$

outer iter. increase

inner iter. decrease

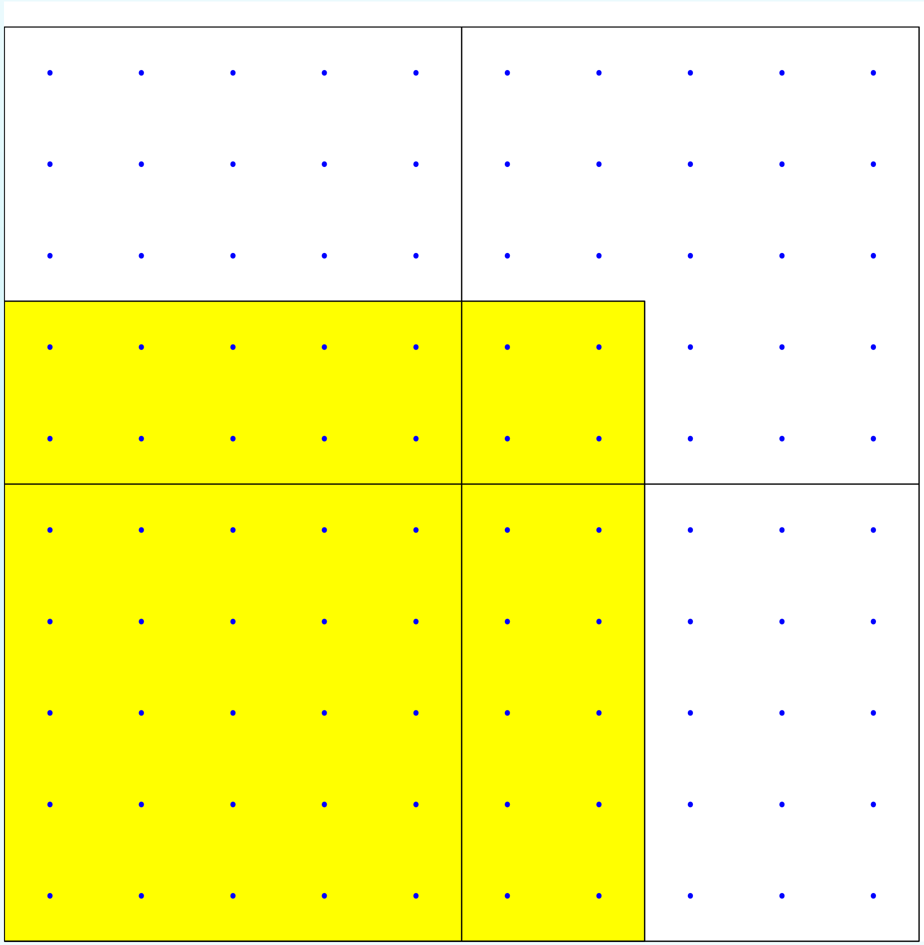
	p = 1	p = 4	p = 25
RILU	160	341	437

Wall clock time

Fixed grid 300×300, strong scalability

	p = 1	p = 4	p = 25
RILU	119	65	15

Overlapping subdomains



Subdomain Ω_1^* for $n_{over} = 2$ n_{over} is the number of overlapping grid points

Overlapping preconditioner

given r, approximate $v = K^{-1}r$

1. r_m^* = restrict r to Ω_m^*,
2. solve $A_{mm}^* v_m^* = r_m^*$ approximately,
3. v_m = restrict v_m^* to Ω_m.

Properties

- The amount of work increases proportional to n_{over}
- The convergence is nearly independent of the subdomain grid size when the physical overlap region is constant

Numerical results

Poisson problem

A_{mm}^{-1} is used in the block preconditioner

3×3 subdomains are used

	overlap		
subgrid size	0	1	2
5×5	10	8	7
10×10	14	9	8
20×20	19	13	10
40×40	26	18	14

Number of iterations

Deflated ICCG

$$x = (I - P^T)x + P^T x$$

$$(I - P^T)x = ZE^{-1}Z^T Ax = ZE^{-1}Z^T b$$

$$AP^T x = PAx = Pb$$

DICCG

$k = 0,\ \hat{r}_0 = Pr_0,\ p_1 = z_1 = L^{-T}L^{-1}\hat{r}_0;$

while $\|\hat{r}_k\|_2 > \varepsilon$ **do**

$k = k + 1;$

$\alpha_k = \frac{(\hat{r}_{k-1}, z_{k-1})}{(p_k, PAp_k)};$

$x_k = x_{k-1} + \alpha_k p_k;$

$\hat{r}_k = \hat{r}_{k-1} - \alpha_k PAp_k;$

$z_k = L^{-T}L^{-1}\hat{r}_k;$

$\beta_k = \frac{(\hat{r}_k, z_k)}{(\hat{r}_{k-1}, z_{k-1})};$ $\quad p_{k+1} = z_k + \beta_k p_k;$

end while

Parallelization of DICCG

Compute and store the sparse vectors

$$c_j = Az_j$$

Compute $E^{-1} = (Z^T AZ)^{-1}$ and store it on each processor
To compute PAv:

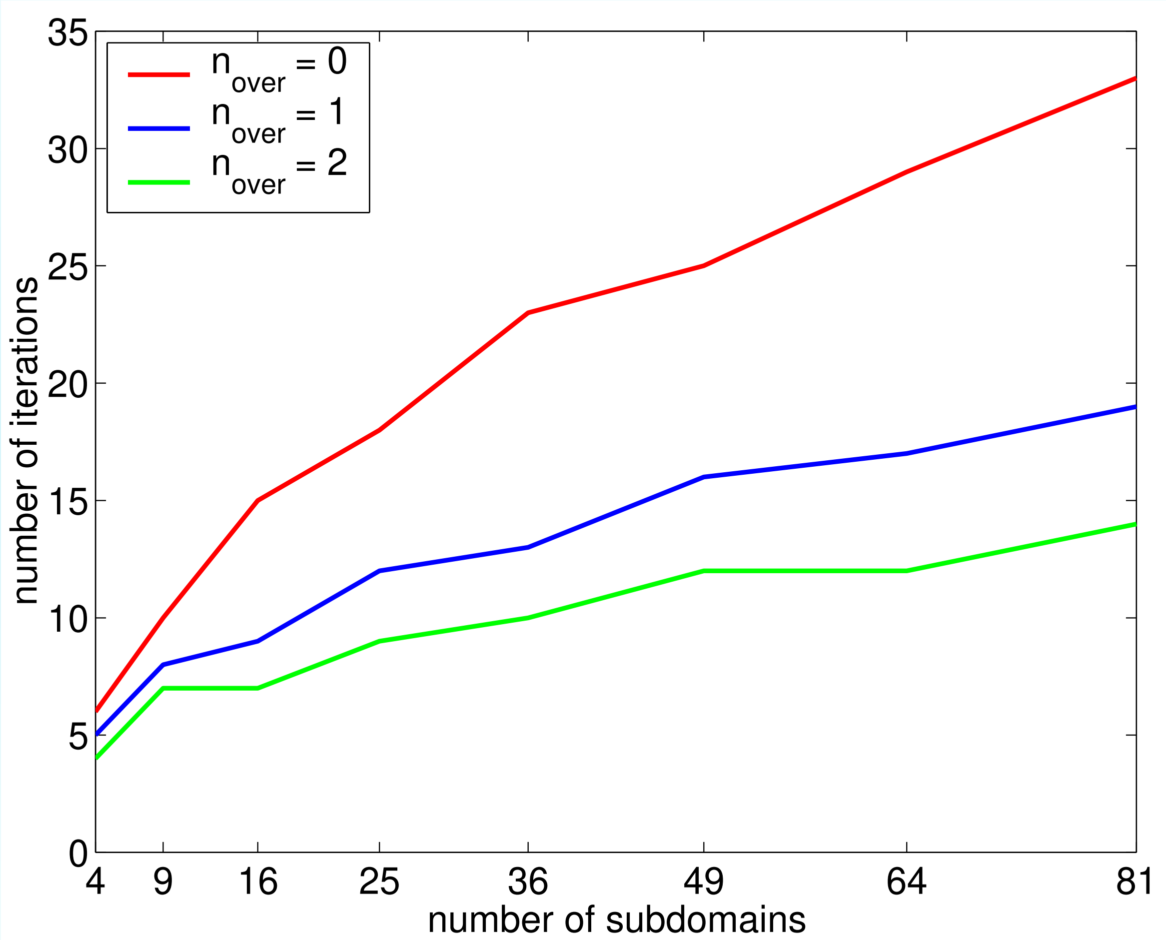
1. $w = Av$

2. Compute the inner products $\tilde{w} = Z^T w$

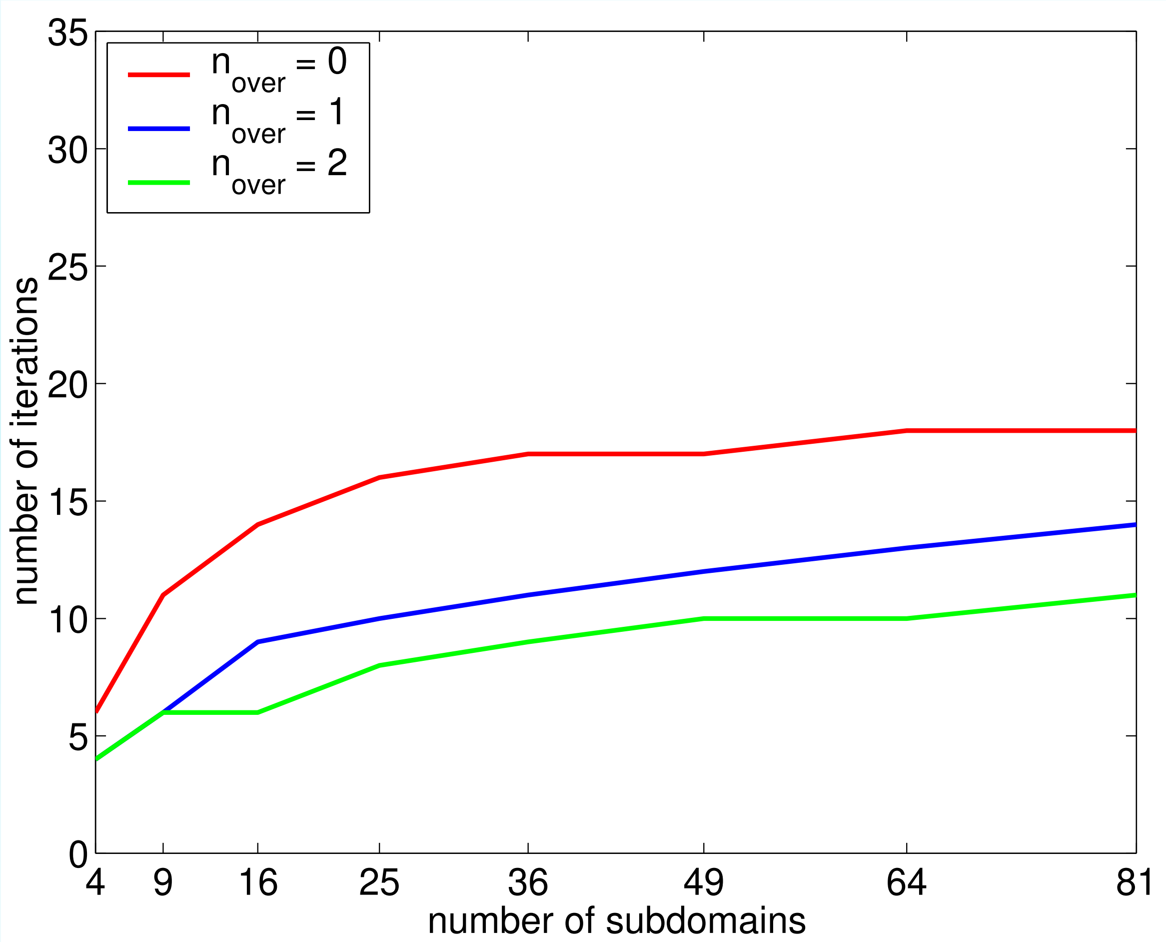
3. $\tilde{e} = (Z^T AZ)^{-1}\tilde{w}$ on each processor

4. form $v - [c_1 ... c_m]\tilde{e}$

Numerical experiments (subgrid 5×5)

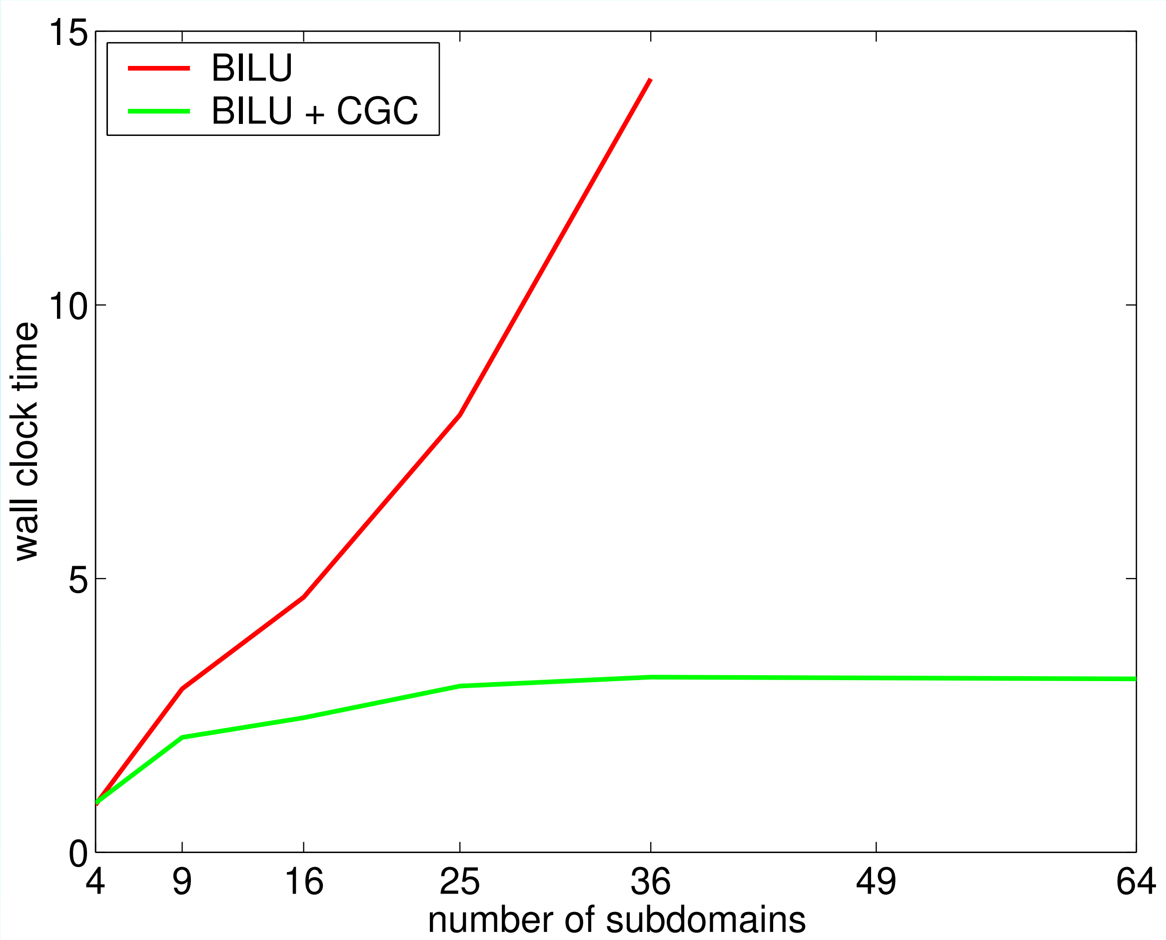


Numerical experiments (subgrid 5×5)



Parallel scalability (weak)

subdomain grid size 50×50 no overlap, wall clock time



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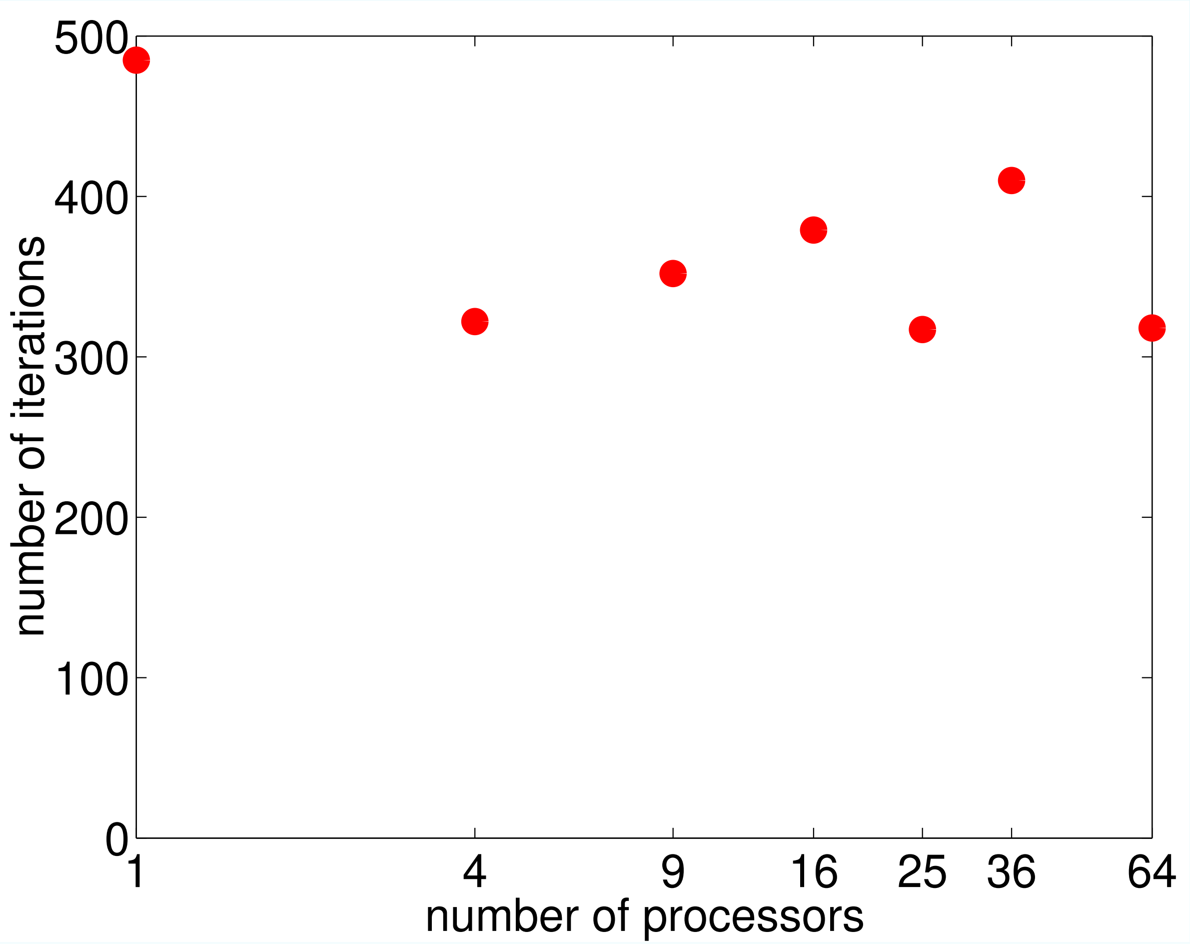
Parallel speedup (strong)

480×480 grid



Parallel speedup (strong)

480×480 grid, Cray T3E